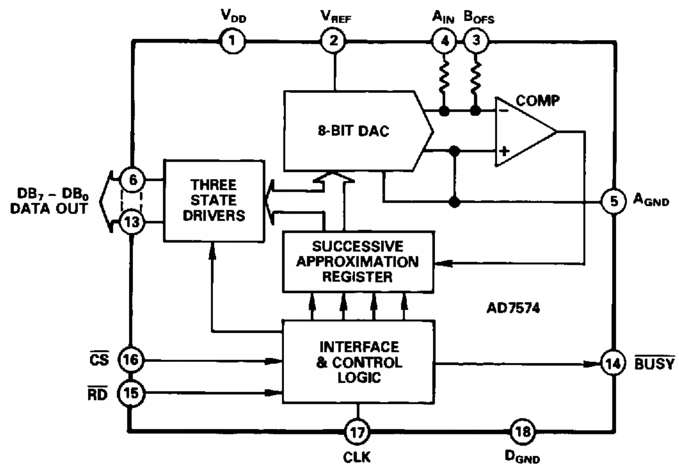
# ANALOG DEVICES

# CMOS µP-Compatible 8-Bit ADC

# AD7574

**FEATURES**
**8-Bit Resolution**
**No Missed Codes over Full Temperature Range**
**Fast Conversion Time: 15µs**
**Interfaces to µP like RAM, ROM or Slow - Memory**
**Low Power Dissipation: 30mW**
**Ratiometric Capability**
**Single +5V Supply**
**Low Cost**
**Internal Comparator and Clock Oscillator**

**FUNCTIONAL BLOCK DIAGRAM**



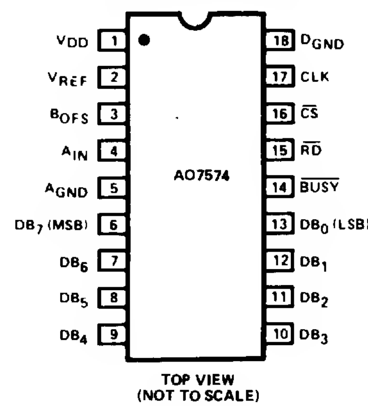

## GENERAL DESCRIPTION

AD7574 is a low-cost, 8-bit µP compatible ADC which uses the successive-approximations technique to provide a conversion time of 15µs.

Designed to be operated as a memory mapped input device, the AD7574 can be interfaced like static RAM, ROM, or slow memory. Its $\overline{CS}$ (decoded device address) and $\overline{RD}$ ($\overline{READ/WRITE}$ control) inputs are available in all µP memory systems. These two inputs control all ADC operations such as starting conversion or reading data. The ADC output data bits use three-state logic, allowing direct connection to the µP data bus or system input port.

Internal clock, +5V operation, on-board comparator and interface logic, as well as low power dissipation (30mW) and fast conversion time make the AD7574 ideal for most ADC/µP interface applications. Small size (18-pin DIP) and monolithic reliability will find wide use in avionics, instrumentation, and process automation applications.

**PIN CONFIGURATION**




**ORDERING GUIDE**

| Model | Temperature Range | Differential Nonlinearity (LSB) | Package Option* |
|---|---|---|---|
| AD7574JN | 0°C to +70°C | ±7/8 max | N-24 |
| AD7574KN | 0°C to +70°C | ±3/4 max | N-24 |
| AD7574AQ | −25°C to +85°C | ±7/8 max | Q-24 |
| AD7574BQ | −25°C to +85°C | ±3/4 max | Q-24 |
| AD7574SQ | −55°C to +125°C | ±7/8 max | Q-24 |
| AD7574TQ | −55°C to +125°C | ±3/4 max | Q-24 |

*N = Plastic DIP; Q = Cerdip.

REV. A



**One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.**
**Tel: 617/329-4700 Fax: 617/326-8703 Twx: 710/394-6577**
**Telex: 924491 Cable: ANALOG NORWOODMASS**

# AD7574—SPECIFICATIONS

## DC SPECIFICATIONS ($V_{DD}$ = +5V, $V_{REF}$ = −10V, Unipolar Configuration, $R_{CLK}$ = 180kΩ, $C_{CLK}$ = 100pF, unless otherwise noted)

| Parameter | Limits $T_A$ = +25°C | Limits $T_{min}$, $T_{max}$[1] | Units | Conditions/Comments |
|---|---|---|---|---|
| ACCURACY | | | | |
| Resolution | 8 | 8 | Bits | |
| Relative Accuracy Error | | | | |
| J, A, S Versions | ±3/4 | ±3/4 | LSB max | Relative Accuracy and Differential Nonlinearity are measured |
| K, B, T Versions | ±1/2 | ±1/2 | LSB max | dynamically using the external clock circuit of Figure 7b. |
| Differential Nonlinearity | | | | Clock frequency is 500kHz (conversion time 15μs). |
| J, A, S Versions | ±7/8 | ±7/8 | LSB max | |
| K, B, T Versions | ±3/4 | ±3/4 | LSB max | |
| Full Scale Error (Gain Error) | | | | Full Scale Error is measured after calibrating out offset error. See |
| J, A, S Versions | ±5 | ±6.5 | LSB max | Figure 8a and associated calibration procedure for offset. Max Full |
| K, B, T Versions | ±3 | ±4.5 | LSB max | Scale change from +25°C to $T_{min}$ or $T_{max}$ is ±2LSB. |
| Offset Error[2] | | | | |
| J, A, S Versions | ±60 | ±80 | mV max | Maximum Offset change from +25°C to $T_{min}$ or $T_{max}$ is ±20mV. |
| K, B, T Versions | ±30 | ±50 | mV max | |
| Mismatch Between $B_{OFS}$ (Pin 3) and $A_{IN}$ (Pin 4) Resistances[3] | ±1.5 | ±1.5 | % max | |
| ANALOG INPUTS | | | | |
| Input Resistance | | | | |
| At $V_{REF}$ (Pin 2) | 5/10/15 | 5/10/15 | kΩ min/typ/max | |
| At $B_{OFS}$ (Pin 3) | 10/20/30 | 10/20/30 | kΩ min/typ/max | |
| At $A_{IN}$ (Pin 4) | 10/20/30 | 10/20/30 | kΩ min/typ/max | |
| $V_{REF}$ (for Specified Performance) | −10 | −10 | V | ±5% for specified transfer accuracy. |
| $V_{REF}$ Range[4] | −5 to −15 | −5 to −15 | V | Degraded transfer accuracy. |
| Nominal Analog Input Range | | | | |
| Unipolar Mode | 0 to +\|$V_{REF}$\| | | V | |
| Bipolar Mode | −\|$V_{REF}$\| to +\|$V_{REF}$\| | | V | |
| LOGIC INPUTS | | | | |
| $\overline{RD}$ (Pin 15), $\overline{CS}$ (Pin 16) | | | | |
| $V_{INH}$ Logic HIGH Input Voltage | +3.0 | +3.0 | V min | |
| $V_{INL}$ Logic LOW input Voltage | +0.8 | +0.8 | V max | |
| $I_{IN}$ Input Current | 1 | 10 | μA max | $V_{IN}$ = 0V, $V_{DD}$ |
| $C_{IN}$ Input Capacitance[5] | 5 | 5 | pF max | |
| CLK (Pin 17) | | | | |
| $V_{INH}$ Logic HIGH Input Voltage | +3.0 | +3.0 | V min | |
| $V_{INL}$ Logic LOW Input Voltage | +0.4 | +0.4 | V max | |
| $I_{INH}$ Logic HIGH Input Current | +2 | +2 | mA max | During Conversion: $V_{IN(CLK)} \geq V_{INH(CLK)}$ |
| $I_{INL}$ Logic LOW Input Current | 1 | 10 | μA max | During Conversion $V_{IN(CLK)} \leq V_{INL(CLK)}$ (see circuit of Figure 7b if external clock operation is required). |
| LOGIC OUTPUTS | | | | |
| BUSY (Pin 14), $DB_7$ to $DB_0$ (Pins 6–13) | | | | |
| $V_{OH}$ Output HIGH Voltage | +4.0 | +4.0 | V min | $I_{SOURCE}$ = 40μA |
| $V_{OL}$ Output LOW Voltage | +0.4 | +0.8 | V max | $I_{SINK}$ = 1.6mA |
| $I_{LKG}$ $DB_7$ to $DB_0$ Floating Stage Leakage | 1 | 10 | μA max | $V_{OUT}$ = 0V or $V_{DD}$ |
| Floating State Output Capacitance ($DB_7$ to $DB_0$)[5] | 7 | 7 | pF max | |
| Output Code | Unipolar Binary, Offset Binary | | | See Figures 8a, 9a, 10a, and 8b, 9b, 10b. |
| POWER REQUIREMENTS | | | | |
| $V_{DD}$ | +5 | +5 | V | ±5% for specified performance. |
| $I_{DD}$ (STANDBY) | 5 | 5 | mA max | $A_{IN}$ = 0V, ADC in RESET condition. |
| $I_{REF}$ | $V_{REF}$ divided by 5kΩ | | max | Conversion complete, prior to RESET. |

NOTES

[1]Temperature ranges as follows: J, K, Versions, 0°C to +70°C; A, B Versions, −25°C to +85°C; S, T Versions; −55°C to +125°C.

[2]Typical offset temperature coefficient is ±150μV/°C.

[3]$R_{BOFS}/R_{AIN}$ mismatch causes transfer function rotation about positive Full Scale. The effect is an offset and a gain term when using the circuit of Figure 9a.

[4]Typical value, not guaranteed or subject to test.

[5]Guaranteed but not tested.

Specifications subject to change without notice.

### CAUTION

ESD (electrostatic discharge) sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.

## AC SPECIFICATIONS ($V_{DD}$ = +5V, $C_{CLK}$ = 100pF, $R_{CLK}$ = 180kΩ unless otherwise noted)

| Symbol | Specification | Limit at $T_A$ = +25°C | Limit at $T_A = T_{min}$ | Limit at $T_A = T_{max}$ | Conditions |
|---|---|---|---|---|---|
| STATIC RAM INTERFACE MODE (See Figure 1 and Table I) | | | | | |
| $t_{CS}$ | CS Pulse Width Requirement | 100ns min | 150ns min | 150ns min | |
| $t_{WSCS}$ | RD to CS Setup Time | 0 min | 0 min | 0 min | |
| $t_{CBPD}$ | CS to BUSY Propagation Delay | 90ns typ | 70ns typ | 150ns typ | BUSY Load = 20pF |
| | | 120ns max | 120ns max | 180ns max | |
| | | 120ns type | 100ns typ | 180ns typ | BUSY Load = 100pF |
| | | 150ns max | 150ns max | 200ns max | |
| $t_{BSR}$ | BUSY to RD Setup Time | 0 min | 0 min | 0 min | |
| $t_{BSCS}$ | BUSY to CS Setup Time | 0 min | 0 min | 0 min | |
| $t_{RAD}$ | Data Access Time | 120ns typ | 100ns typ | 180ns typ | $DB_0$–$DB_7$ Load = 100pF |
| | | 150ns max | 150ns max | 220ns max | |
| | | 240ns typ | 220ns typ | 300ns typ | $DB_0$–$DB_7$ Load = 100pF |
| | | 300ns max | 300ns max | 400ns max | |
| $t_{RHD}$ | Data Hold Time | 80ns typ | 40ns typ | 120ns typ | |
| | | 50ns min | 30ns min | 80ns min | |
| | | 120ns max | 80ns max | 180ns max | |
| $t_{RHCS}$ | CS to RD Hold Time | 250ns max | 200 ns max | 500ns max | |
| $t_{RESET}$ | Reset Time Requirement | 3µs min | 3µs min | 3µs min | |
| $t_{CONVERT}$ | Conversion Time Using Internal Clock Oscillator | See Typical Data of Figure 7a | | | |
| $t_{CONVERT}$ | Conversion Time Using External Clock | 15µs | 15µs | 15µs | $f_{CLK}$ = 500kHz Circuit of Figure 7b |
| ROM INTERFACE MODE (See Figure 2 and Table II) | | | | | |
| $t_{RAD}$ | Data Access Time | Same as RAM Mode | | | |
| $t_{RHD}$ | Data Hold Time | Same as RAM Mode | | | |
| $t_{WBPD}$ | RD HIGH to BUSY Propagation Delay | 400ns typ 1.5µs | 350ns typ 1.0µs | 1µs typ 2.0µs | BUSY Load = 20 pF |
| $t_{BSR}$ | BUSY to RD LOW Setup Time | RD can go LOW prior to BUSY = HIGH, but must not return HIGH until = BUSY HIGH. See Table II. | | | |
| $t_{CONVERT}$ | Conversion Time Using Internal Clock Oscillator | See Typical data of Figure 7a. Add 2µs to data shown in Figure 7a for ROM Mode | | | |
| SLOW – MEMORY INTERFACE MODE (See Figure 3 and Table III) | | | | | |
| $t_{CBPD}$ | CS to BUSY Propagation Delay | Same as RAM Mode | | | |
| $t_{RESET}$ | Reset Time Requirement | Same as RAM Mode | | | |
| $t_{RAD}$ | Data Access Time | Same as RAM Mode | | | |
| $t_{RHD}$ | Data Hold Time | Same as RAM Mode | | | |
| $t_{CONVERT}$ | Conversion Time | Same as RAM Mode | | | |

**ABSOLUTE MAXIMUM RATINGS***

$V_{DD}$ to $A_{GND}$ . . . . . . . . . . 0V, +7.0V
$V_{DD}$ to $D_{GND}$ . . . . . . . . . . 0V, +7.0V
$A_{GND}$ to $D_{GND}$ . . . . . . . . . . −0.3V, $V_{DD}$
Digital Input Voltage to $D_{GND}$ (Pins 15 and 16) . . . . −0.3V, +15.0V
Digital Output Voltage to $D_{GND}$ (Pins 6–14) . . . . . . . . −0.3V, $V_{DD}$
CLK Input Voltage (Pin 17) to$D_{GND}$ . . . . . . . . −0.3V, $V_{DD}$
$V_{REF}$ (Pin 2) . . . . . . . . . . ±20V
$V_{BOFS}$ (Pin 3) . . . . . . . . . . ±20V
$V_{AIN}$ (Pin 4) . . . . . . . . . . ±20V
Operating Temperature Range
Commercial (J, K Versions) . . . . . . . . 0°C to +70°C
Industrial (A, B Versions) . . . . . . . . −25°C to +85°C
Extended (S, T Versions) . . . . . . . . −55°C to +150°C
Storage Temperature Range . . . . . . . . −65°C to +150°C
Lead Temperature (soldering, 10 secs) . . . . . . . . +300°CV
Power Dissipation (Package)
Plastic (Suffix N)
to +70°C . . . . . . . . . . 670mW
Derate above +70°C by . . . . . . . . 8.3mW/°C
Cerdip (Suffix Q)
to +75°C . . . . . . . . . . 450mW
Derate above +75°C by . . . . . . . . 6mW/°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to above maximum rating conditions for extended periods may affect device reliability.

## TERMINOLOGY

**RESOLUTION:** Resolution is a measure of the *nominal* analog change required for a 1-bit change in the A/D converter's digital output. While normally expressed in a number of bits, the analog resolution of an n-bit unipolar A/D converter is $(2^{-n})$ $V_{REF}$). Thus, the AD7574, an 8-bit A/D converter, can resolve analog voltages as small as (1/256) ($V_{REF}$) when operated in a unipolar mode. When operated in a bipolar mode, the resolution is (1/128) ($V_{REF}$). Resolution does not imply accuracy. *Usable* resolution is limited by the differential nonlinearity of the A/D converter.

**RELATIVE ACCURACY:** Relative accuracy is the deviation of the ADC's actual code transition points from a straight line drawn between the devices' measured zero and measured full scale transition points. Relative accuracy, therefore, is a measure of code *position.*

**DIFFERENTIAL NONLINEARITY:** Differential nonlinearity in an ADC is a measure of the size of an anlog voltage range associated with any digitial output code. As such, differential nonlinearity specifies code width (usable resolution). An ADC with a specified differential nonlinearity of ±n bits will exhibit codes ranging in width from 1LSB −n LSB to 1LSB +n LSB. A specified differential nonlinearity of less than ±1LSB guarantees no-missing-codes operation.

## TIMING & CONTROL OF THE AD7574

### STATIC RAM INTERFACE MODE

Table I and Figure 1 show the truth table and timing requirements for AD7574 operation as a static RAM.

A convert start is initiated by executing a memory WRITE instruction to the address location occupied by the AD7574 (once conversion has started, subsequent memory WRITES have no effect). A data READ is performed by executing a memory READ instruction to the AD7574 address location.

$\overline{BUSY}$ must be HIGH before a data READ is attempted, i.e. the total delay between a convert start and a data READ must be at least as great as the AD7574 conversion time. The delay can be generated by inserting NOP instructions (or other program instructions) between the WRITE (start convert) and READ (read data) operations. Once $\overline{BUSY}$ is HIGH (conversion complete), a data READ is performed by executing a memory READ instruction to the address location occupied by the AD7574. The data readout is destructive, i.e. when RD returns HIGH, the converter is internally reset.

The RAM interface mode uses distinctly different commands to start conversion (memory WRITE) or read the data (memory READ). This is in contrast to the ROM mode where a memory READ causes a data READ *and* a conversion restart.

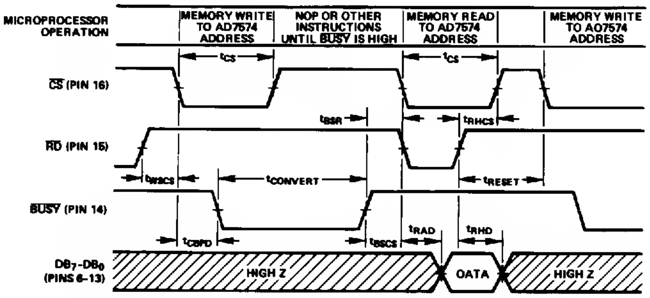



*Figure 1. Static RAM Mode Timing Diagram*

*Table I. Truth Table, Static RAM Mode*

| AD7574 INPUTS | | AD7574 OUTPUTS | | AD7574 OPERATION |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{RD}$ | $\overline{BUSY}$ | $DB_7$-$DB_0$ | |
| L | H | H | HIGH Z | WRITE CYCLE (START CONVERT) |
| L | ↓ | H | HIGH Z → DATA | READ CYCLE (DATA READ) |
| L | ↑ | H | DATA → HIGH Z | RESET CONVERTER |
| H | X[1] | X | HIGH Z | NOT SELECTED |
| L | H | L | HIGH Z | NO EFFECT, CONVERTER BUSY |
| L | ↓ | L | HIGH Z | NO EFFECT, CONVERTER BUSY |
| L | ↑ | L | HIGH Z | NOT ALLOWED, CAUSES INCORRECT CONVERSION |

Note 1: If $\overline{RD}$ goes LOW to HIGH when $\overline{CS}$ is LOW, the ADC is internelly reset. $\overline{RD}$ has no effect while $\overline{CS}$ is HIGH. See application hint No. 1.

### ROM INTERFACE MODE

Table II and Figure 2 show the truth table and timing requirements for interfacing the AD7574 like Read Only Memory.

$\overline{CS}$ is held LOW and converter operation is controlled by the $\overline{RD}$ input. The AD7574 $\overline{RD}$ input is derived from the decoded device address. MEMRD should be used to enable the address decoder in 8080 systems. VMA should be used to enable the address decoder in 6800 systems. A data READ is initiated by executing a memory READ instruction to the AD7574 address location. The converter is automatically restarted when $\overline{RD}$ returns HIGH. As in the RAM mode, attempting a data READ before $\overline{BUSY}$ is HIGH will result in incorrect data being read.

The advantage of the ROM mode is its simplicity. The major disadvantage is that the data obtained is relatively poorly defined in time inasmuch as executing a data READ automatically starts a new conversion. This problem can be overcome by executing two READs separated by NO-OPS (or other program instructions) and using only the data obtained from the second READ.

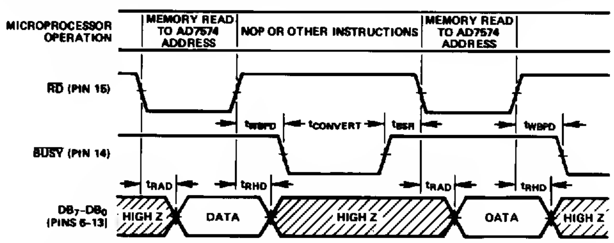



*Figure 2. ROM Mode Timing Diagram ($\overline{CS}$ Held LOW)*

*Table II. Truth Table, ROM Mode*

| AD7574 INPUTS | | AD7574 OUTPUTS | | AD7574 OPERATION |
|---|---|---|---|---|
| $\overline{CS}$ | $\overline{RD}$ | $\overline{BUSY}$ | $DB_7$-$DB_0$ | |
| L | ↓ | H | HIGH Z → DATA | DATA READ |
| L | ↑ | ↓ | DATA → HIGH Z | RESET AND START NEW CONVERSION |
| L | ↓ | L | HIGH Z | NO EFFECT, CONVERTER BUSY |
| L | ↑ | L | HIGH Z | NOT ALLOWED, CAUSES INCORRECT CONVERSION |

### SLOW-MEMORY INTERFACE MODE

Table III and Figure 3 show the truth table and timing requirements for interfacing the AD7574 as a slow-memory. This mode is intended for use with processors which can be forced into a WAIT state for at least 12μs (such as the 8080, 8085 and SC/MP). The major advantage of this mode is that it allows the μP to start conversion, WAIT, and then READ data with a single READ instruction.

In the slow-memory mode, $\overline{CS}$ and $\overline{RD}$ are tied together. It is suggested that the system ALE signal (8085 system) or SYNC signal (8080 system) be used to latch the address. The decoded device address is subsequently used to drive the AD7574 $\overline{CS}$ and $\overline{RD}$ inputs. $\overline{BUSY}$ is connected to the microprocessor READY input.

When the AD7574 is NOT addressed, the $\overline{CS}$ and $\overline{RD}$ inputs are HIGH. Conversion is initiated by executing a memory READ to the AD7574 address. $\overline{BUSY}$ subsequently goes LOW (forcing the μP READY input LOW) placing the μP in a WAIT state. When conversion is complete ($\overline{BUSY}$ is HIGH) the μP completes the memory READ.

Do not attempt to perform a memory WRITE in this mode, since three-state bus conflicts will arise.

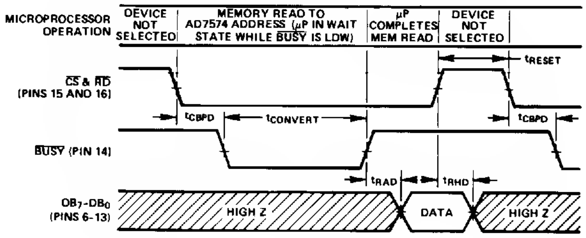



*Figure 3. Slow Memory Mode Timing Diagram ($\overline{CS}$ and $\overline{RD}$ Tied Together)*

*Table III. Truth Table, Slow Memory Mode*

| AD7574 INPUTS | AD7574 OUTPUTS | | AD7574 OPERATION |
|---|---|---|---|
| $\overline{CS}$ & $\overline{RD}$ | $\overline{BUSY}$ | $DB_7$ - $DB_0$ | |
| H | H | HIGH Z | NOT SELECTED |
| ↓ | H→L | HIGH Z | START CONVERSION |
| L | L | HIGH Z | CONVERSION IN PROGRESS, µP IN WAIT STATE |
| L | ↑ | HIGH Z → DATA | CONVERSION COMPLETE, µP READS DATA |
| ↑ | H | DATA → HIGH Z | CONVERTER RESET AND DESELECTED |
| H | H | HIGH Z | NOT SELECTED |

## GENERAL CIRCUIT INFORMATION

### BASIC CIRCUIT DESCRIPTION

The AD7574 uses the successive approximations technique to provide an 8-bit parallel digital output. The control logic was designed to provide easy interface to most microprocessors. Most applications require only passive clock components (R & C), a -10V reference, and +5V power.

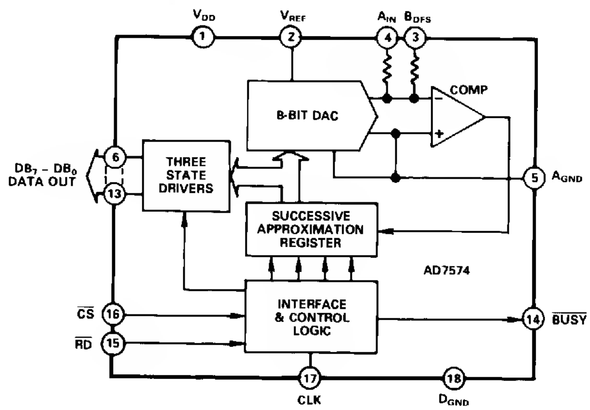



*Figure 4. AD7574 Functional Diagram*

Figure 4 shows the AD7574 functional diagram. Upon receipt of a start command either via the $\overline{CS}$ or $\overline{RD}$ pins, $\overline{BUSY}$ goes low indicating conversion is in progress. Successive bits, starting with the most significant bit (MSB) are applied to the input of a DAC. The comparator determines whether the addition of each successive bit causes the DAC output to be greater than or less than the analog input, $A_{IN}$. If the sum of the DAC bits is less than $A_{IN}$, the trial bit is left ON, and the next smaller bit is tried. If the sum is greater than $A_{IN}$, the trial bit is turned OFF and the next smaller bit is tried.

Each successively smaller bit is tried and compared to $A_{IN}$ in this manner until the least significant bit (LSB) decision has been made. At this time $\overline{BUSY}$ goes HIGH (conversion is complete) indicating the successive approximation register contains a valid representation of the analog input. The $\overline{RD}$ control (see the previous page for details) can then be exercised to activate the three-state buffers, placing data on the $DB_0$ - $DB_7$ data output pins. $\overline{RD}$ returning HIGH causes the clock oscillator to run for 1 cycle, providing an internal ADC reset (i.e. the SAR is loaded with code 10000000).

### DAC CIRCUIT DETAILS

The current weighting D/A converter is a precision multiplying DAC. Figure 5 shows the functional diagram of the DAC as used in the AD7574. It consists of a precision Silicon Chromium thin film R/2R ladder network and 8 N-channel MOSFET switches operated in single-pole-double-throw.

The currents in each 2R shunt arm are binarily weighted, i.e. the current in the MSB arm is $V_{REF}$ divided by 2R, in the second arm is $V_{REF}$ divided by 4R, etc. Depending on the DAC logic input (A/D output) from the successive approximation register, the current in the individual shunt arms is steered either to $A_{GND}$ or to the comparator summing point.

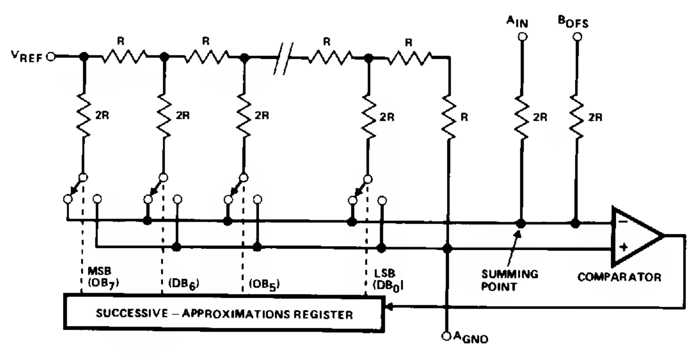



*Figure 5. D/A Converter As Used In AD7574*

# OPERATING THE AD7574

## APPLICATION HINTS

1. TIMING & CONTROL
   In the AD7574 when a conversion is finished the fresh data must be read before a new conversion can be started.
   Failure to observe the timing restrictions of Figures 1, 2 or 3 may cause the AD7574 to change interface modes. For example, in the RAM mode, holding $\overline{CS}$ LOW too long after $\overline{RD}$ goes HIGH will cause a new convert start (i.e. the converter moved into the ROM mode).
2. LOGIC DEGLITCHING IN uP APPLICATIONS
   Unspecified states on the address bus (due to different rise and fall times on the address bus) can cause glitches at the AD7574 $\overline{CS}$ or $\overline{RD}$ terminals. These glitches can cause unwanted convert starts, reads, or resets. The best way to avoid glitches is to gate the address decoding logic with RD or WR (8080) or VMA (6800) when in the ROM or RAM mode. When in the slow-memory mode, the ALE (8085) or SYNC (8080) signal should be used to latch the address.
3. INPUT LOADING AT $V_{REF}$, $A_{IN}$ AND $B_{OFS}$
   To prevent loading errors due to the finite input resistance at the $V_{REF}$, $A_{IN}$ or $B_{OFS}$ pins, low impedance driving sources must be used (i.e. op amp buffers or low output-Z reference).
4. RATIOMETRIC OPERATION
   Ratiometric performance is inherent to A/D converters such as the AD7574 which use a multiplying DAC weighting network. However, the user should recognize that comparator limitations such as offset voltage, input noise and gain will cause degradation of the transfer characteristics when operating with reference voltages less than -10V in magnitude.
5. OFFSET CORRECTION
   Offset error in the transfer characteristic can be trimmed by offsetting the buffer amplifier which drives the AD7574 $A_{IN}$ pin (pin 4). This can be done either by summing a cancellation current into the amplifier's summing junction, or by tapping a voltage divider which sits between $V_{DD}$ and $V_{REF}$ and applying the tap voltage to the amplifier's positive input (an example of a resistive tap offset adjust is shown in Figure 10a where $R_8$, $R_9$ and $R_{10}$ can be used to offset the ADC).
6. ANALOG AND DIGITAL GROUND
   It is recommended that $A_{GND}$ and $D_{GND}$ be connected locally to prevent the possibility of injecting noise into the AD7574. In systems where the $A_{GND}$-$D_{GND}$ intertie is not local, connect back-to-back diodes (IN914 or equivalent) between the AD7574 $A_{GND}$ and $D_{GND}$ pins.
7. INITIALIZATION AFTER POWER – UP
   Execute a memory READ to the AD7574 address location, and subsequently ignore the data. The AD7574 is internally reset when reading out data, i.e. the data readout is destructive.

### CLOCK OSCILLATOR

The AD7574 has an internal asynchronous clock oscillator which starts upon receipt of a convert start command, and ceases oscillating when conversion is complete.

The clock oscillator requires an external R and C as shown in Figure 6. Nominal conversion times versus $R_{CLK}$ and $C_{CLK}$ is shown in Figure 7a. The curves shown in Figure 7a are applicable when operating in the RAM or slow-memory interface modes. When operating in the ROM interface mode, add 2μs to the typical conversion time values shown.

The AD7574 is guaranteed to provide transfer accuracy to published specifications for conversion times down to 15μs, as indicated by the unshaded region of Figure 7a. Conversion times faster than 15μs can cause transfer accuracy degradation.

### OPERATION WITH EXTERNAL CLOCK

For applications requiring a conversion time close to or equal to 15μs, an external clock is recommended. Using an external clock precludes the possibility of converting faster than 15μs (which can cause transfer accuracy degradation) due to temperature drift – as may be the case when using the internal clock oscillator.

Figure 7b shows how the external clock must be connected. The $\overline{BUSY}$ output of the AD7574 is connected to the three-state enable input of a 74125 three-state buffer. $R_1$ is used as a pullup, and can be between 6kΩ and 100kΩ. A 500kHz clock will provide a conversion time of 15μs.

The external clock should be used only in the static-RAM or slow-memory interface mode, and *not* in the ROM mode.

Timing constraints for external clock operation are as follows:

STATIC RAM MODE

1. When initiating a conversion, $\overline{CS}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.
2. A data READ can be initiated any time after $\overline{BUSY}$ = 1.

SLOW-MEMORY MODE

1. When initiating a conversion, $\overline{CS}$ and $\overline{RD}$ should go LOW on a positive clock edge to provide optimum settling time for the MSB.

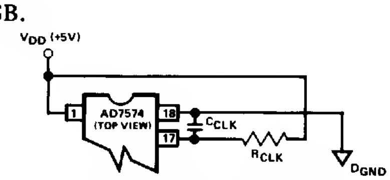



*Figure 6. Connecting $R_{CLK}$ and $C_{CLK}$ To CLK Oscillator*

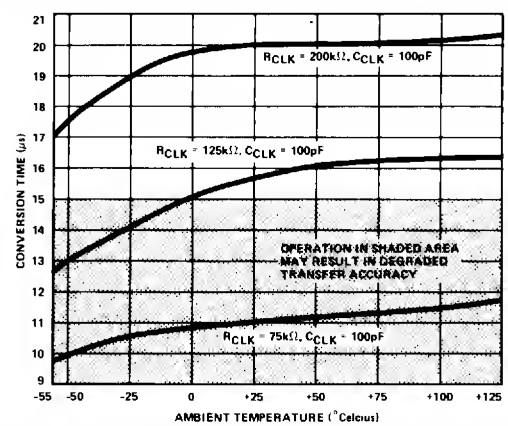



*Figure 7a. Typical Conversion Time vs. Temperature For Different $R_{CLK}$ and $C_{CLK}$ (Applicable to RAM and Slow-Memory Modes. For ROM Mode add 2μs to values shown)*

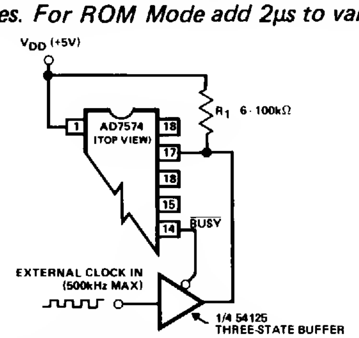



*Figure 7b. External Clock Operation (Static RAM and Slow-Memory Mode)*

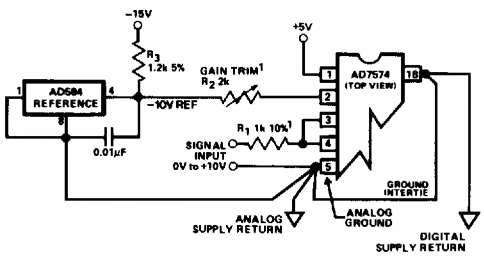
### UNIPOLAR BINARY OPERATION

Figures 8a and 8b show the analog circuit connections and typical transfer characteristic for unipolar operation. An AD584 is used as the -10V reference.

Calibration is as follows:

OFFSET

Offset must be trimmed out in the signal conditioning circuitry used to drive the signal input terminals shown in Figure 8a. An example of an offset trim is shown in Figure 10a, where $R_8$, $R_9$ and $R_{10}$ comprise a simple voltage tap which is applied to the amplifier's positive input.




Note 1: $R_1$ and $R_2$ can be omitted if gain trim is not required

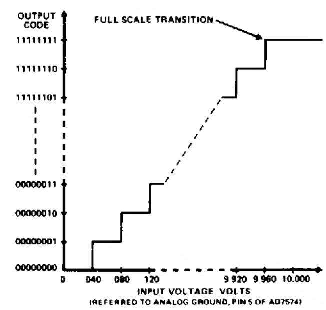
*Figure 8a. AD7574 Unipolar (0V to +10V) Operation (Output Code is Straight Binary)*

1. Apply -39.1mV (1 LSB) to the input of the buffer amplifier used to drive $R_1$ (i.e. +39.1mV at $R_1$).
2. While performing continuous conversions, adjust the offset potentiometer (described above) until $DB_7$ - $DB_1$ are LOW and the LSB ($DB_0$) flickers.

GAIN (FULL SCALE)

Offset adjustment must be performed before gain adjustment.

1. Apply -9.961V to the input of the buffer amplifier used to drive $R_1$ (i.e. +9.961V at $R_1$).
2. While performing continuous conversions, adjust trim pot $R_2$ until $DB_7$ - $DB_1$ are HIGH and the LSB ($DB_0$) flickers.




Note: Approximate bit weights are shown for illustration. Nominal bit weight for a -10V reference is ≈ 39.1mV

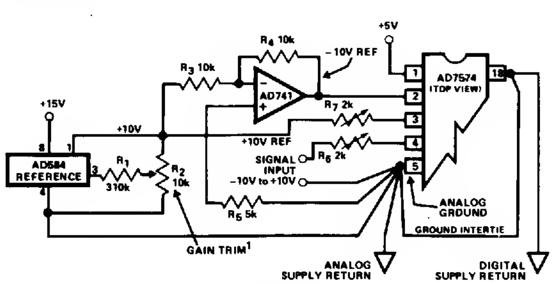
*Figure 8b. Nominal Transfer Characteristic For Unipolar Circuit of Figure 8a*

### BIPOLAR (OFFSET BINARY) OPERATION

Figures 9a and 9b illustrate the analog circuitry and transfer characteristic for bipolar operation. Output coding is offset binary. As in unipolar operation, offset correction can be performed at the buffer amplifier used to drive the signal input terminals of Figure 9a (Resistors $R_8$, $R_9$ and $R_{10}$ in Figure 10a show how offset trim can be done at the buffer amplifier).

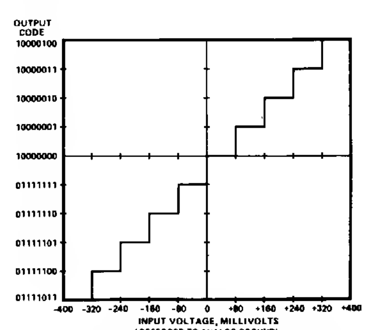
Calibration is as follows:

1. Adjust $R_6$ and $R_7$ for minimum resistance across the potentiometers.
2. Apply +10.000V to the buffer amplifier used to drive the signal input (i.e. -10.000V at $R_6$).
3. While performing continuous conversions, trim $R_6$ or $R_7$ (whichever required) until $DB_7$ - $DB_1$ are LOW and the LSB ($DB_0$) flickers.
4. Apply 0V to the buffer amplifier used to drive the signal input terminals.
5. Doing continuous conversions, trim the offset circuit of the buffer amplifier until the ADC output code flickers between 01111111 and 10000000.
6. Apply +10.000V to the input of the buffer amplifier (i.e. -10.000V as applied to $R_6$).
7. Doing continuous conversions, trim $R_2$ until $DB_7$ - $DB_1$ are LOW and the LSB ($DB_0$) flickers.
8. Apply -9.922V to the input of the buffer amplifier (i.e. +9.922V at the input side of $R_6$).
9. If the ADC output code is not 11111110 ±1 bit, repeat the calibration procedure.




Note 1: $R_1$ and $R_2$ can be omitted if gain trim is not required

*Figure 9a. AD7574 Bipolar (-10V to +10V) Operation (Output Code is Offset Binary)*




Note: Approximate bit weights are shown for illustration. Nominal bit weight for ± 10V full scale is ≈ 78.1mV

*Figure 9b. Nominal Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 9a*

# OPERATING THE AD7574

## BIPOLAR (COMPLEMENTARY OFFSET BINARY) OPERATION

Figure 10a shows the analog connections for complementary offset binary operation. The typical transfer characteristic is shown in Figure 10b. In this bipolar mode, the ADC is fooled into believing it is operated in a unipolar mode - i.e. the +10V to −10V analog input is conditioned into a 0 to +10V signal range. $R_2$ is the gain adjust, while $R_9$ is the offset adjust.

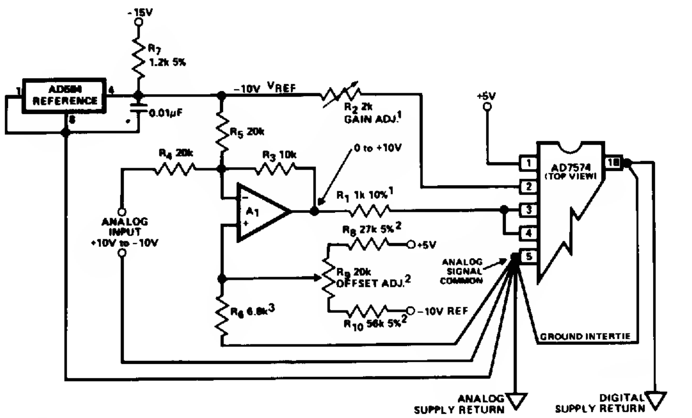
Calibration is as follows (adjust offset before gain):

OFFSET

1. Apply OV to the analog input shown in Figure 10a.
2. While performing continuous conversions, adjust $R_9$ until the converter output flickers between codes 01111111 and 10000000.

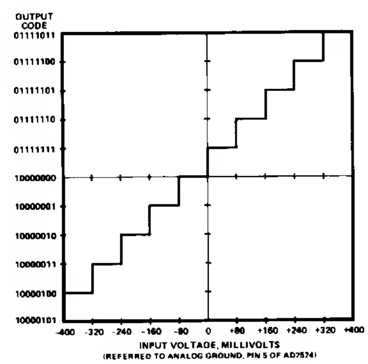
GAIN (FULL SCALE)

1. Apply −9.922V across the analog input terminals shown in Figure 10a.
2. While performing continuous conversions, adjust $R_2$ until $DB_7$ - $DB_1$ are HIGH and the LSB ($DB_0$) flickers between HIGH and LOW.




Notes:
1. $R_1$ and $R_2$ can be omitted if gain trim is not required
2. $R_8$, $R_9$ and $R_{10}$ can be omitted if offset trim is not required
3. $R_6 \| R_8 \| R_{10}$ = 5kΩ. If $R_8$, $R_9$ and $R_{10}$ not used, make $R_6$ = 5kΩ

*Figure 10a. AD7574 Bipolar Operation (−10V to +10V) (Output Code is Complementary Offset Binary)*




Note: Approximate bit weights are shown for illustration. Nominal bit weight for ±10V full scale is ≈ 78.1mV

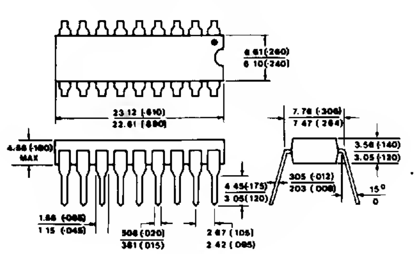
*Figure 10b. Nominal Transfer Characteristic Around Major Carry for Bipolar Circuit of Figure 10a*

# MECHANICAL INFORMATION

## OUTLINE DIMENSIONS

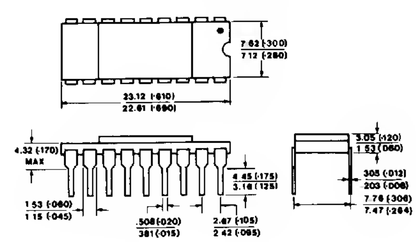
Dimensions are shown in inches and (mm).

### 18 PIN PLASTIC DIP



Notes:
1. Lead no.1 identified by dot or notch.
2. Dimensions in mm (in.).
3. Leads are solder plated KOVAR or ALLOY 42.

### 18 PIN CERAMIC DIP



Notes:
1. Lead no. 1 identified by dot or notch.
2. Leads will be either gold or tin plated in accordance with MIL-M-38510 requirements.
3. Cavity lid is electrically isolated.

C505d–5–6/85

PRINTED IN U.S.A.